REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-15 and 19-24 are presently active.

In the Office Action, Claims 2, 13, and 14 were objected to for failing to further limit the subject matter of a previous claim. Claims 1, 2, 8-12, and 15 were rejected under U.S.C. § 102(b) as being anticipated by Dreifus et al (U.S. Pat. No. 5,173,761). Claims 4, 13, and 14 were rejected under U.S.C. § 103(a) as being unpatentable over Dreifus et al. Claims 3, 5-7, and 19-24 were indicated as being allowed.

Applicants acknowledge with appreciation the indication of allowance for Claims 3, 5-7, and 19-24. However, Applicants submit that the other claims are likewise allowable for the following reasons.

M.P.E.P. § 2131 requires for anticipation that each and every feature of the claimed invention must be shown in as complete detail as is contained in the claim. The Court in *Net Moneyin, Inc. v. Versigen, Inc.*, 454 F.3d 1359, 1371, 88 USPQ2d 1751, 1760 (Fed. Circ. 2008) explained that:

> Rejections under 35 U.S.C. §102 are proper only when the claimed subject matter is identically disclosed or described in the prior art. Thus, it is not enough that the prior art reference discloses part of the claimed invention, which an ordinary artisan might supplement to make the whole, or that it includes multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention. The prior art reference must ***clearly and unequivocally disclose the claimed invention*** or direct those skilled in the art to the invention without any need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference. [Emphasis added.]

Claim 1 recites:

> 1. A microelectrode comprising:
> an electrically conducting diamond layer;
> a non-conducting diamond layer formed from electrically non-conducting diamond presenting a planar surface;

> one or more pins or projections of electrically conducting diamond extending at least partially through the non-conducting diamond layer, the pins or projections presenting planar areas of electrically conducting diamond;
> the pins or projections which extend to the planar surface of the non-conducting diamond layer, presenting one or more planar areas of electrically conducting diamond co-planar with the planar surface of the electrically non-conducting diamond; and
> a contact surface or surfaces on a back side of the electrically conducting diamond layer for connection to an external circuit.

The embodiment illustrated in Figure 1 and described in col. 2, line 67, to col. 3, line 47, of Dreifus et al will not function as a microelectrode as there is no electrical contact (at any of the steps) between the front of the structure and the back of the structure because there is an intrinsic diamond layer 20, i.e. non-conducting layer, disposed between the silicon substrate 10 and the B-doped layer 25.

Claim 1 requires that the back side of the electrically conducting diamond layer has a contact surface or surfaces for connection to an external circuit.

Figure 1 of Dreifus et al does not ***clearly and unequivocally*** have the recited contact surface or surfaces on a back side of the electrically conducting diamond layer.

The other embodiment referred to by the Examiner is illustrated in Figures 4a and 4b of Dreifus et al, and is described in col. 4, line 27, to col. 5, line 24.

To understand Figures 4a and 4b, it is instructive to read the accompanying text as this makes it clear the spatial and dimensional relationships between the various parts of the embodiment. The following is the sequence of steps used to produce the article of Figure 4a and 4b (together with the structural consequence of the step).

1. Start with a 25-30 μm thick polycrystalline layer (col. 4, lines 28-30). This layer is undoped - it is described as '20' referring back to the paragraph bridging col. 2 and col. 3.

2. The channel layer 25 (i.e. the conductive region) is formed by ion implanting into the undoped region (col. 4 line 30 - 34). The highest energy implantation is carbon at an energy of 200 keV (col. 4, lines 53-57). This is the structure that is shown in Figure 4a.
3. Further lower energy implants are made to ensure that the conductive region reaches the surface, the regions 50 in Figure 4b.

The Examiner is suggesting that the implantation process makes the initial 25-30 μm thick insulating diamond layer conductive over its whole thickness (else there would be no possibility of reading out the signal at the rear surface as is required in amended claim 1 of the present application). This would mean that the implanted ions would have to reach a distance of 25-30 μm below the surface.

However, Dreifus et al indicate that the region of conductivity only extends to about 0.1 μm below the surface: col. 4, lines 64-66 "an effective channel carrier concentration of about $1 \times 10^{17}/cm^3$ at a depth of 1000 Å from the surface." Thus, beneath the conductive region there is a region of between 24.9 and 29.9 μm thickness which has not been ion implanted. This region remains in its original form, namely intrinsic diamond which is non-conducting.

The penetration depth of implantations are straight forward to determine using a Monte Carlo simulation (see http://www.srim.org/ for example), such simulations are widely used and have been available as public domain applications since the mid-1980s. The Dreifus et al disclosure is clear - penetration of the ion implantation is to a depth of 1000 Å.

Thus, this embodiment of Dreifus et al does not show any means of electrically connecting the front surface to the back surface as there is an intervening layer of undoped diamond, as in the embodiment of Figure 1.

Hence, Claim 1 is not anticipated by Dreifus et al.

Indeed, Dreifus et al's claims add further support for this argument. Both of their independent claims 1 and 2 require the presence of a layer of insulating diamond.

Dreifus et al require the presence of an insulating diamond layer of at least 20 microns thick between the conducting diamond layer and the substrate. Figure 1 of Dreifus et al illustrate a diode. In such a diode a current flow perpendicular to the layers of a diamond and therefore needs to have an insulating layer present between the conducting layer and the conducting substrate. If there was no insulating layer, current would flow in either direction and it would not have the characteristics of a diode (i.e. blocks current flow in one direction).

Figure 4b is a step in the production of a transistor structure. The current flow in this transistor structure is along the 'channel' between the source and the drain contacts (regions 50 in Figure 4b) and is therefore more-or-less parallel to the surface. The current flow through the channel of p-type doped conductive material can be 'pinched-off' by applying a voltage to the gate electrode (and thereby producing an electric field underneath the gate electrode); this is the essence of the operation of a transistor. In a transistor of this type in diamond, it is necessary to have an insulating layer beneath the channel so that the current can be pinched-off. In the absence of an insulating region, the current path would simply move in response to the electric field beneath the gate electrode, but would still flow from the source to the drain. In other words, there would be no transistor effect in the absence of an insulating region.

Clearly, therefore, Dreifus et al do not provide any teaching or suggestion that the insulating layer should be removed.

Finally, regarding the claim objection, the examiner's attention is invited to notice that Claim 1 defines one or more pins or projections of electrically conducting diamond extending ***at least partially through*** the non-conducting diamond layer, while Claim 2 defines (and is further limiting) in that it defines that the pins or projections ***extend to a surface of the non-conducting diamond layer***. Thus, the claim objection should be removed.

Hence, Claims 1, 2, 4, and 8-15 patentably define over the art and should be passed to allowance.

In light of the above discussion, the application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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